PATENT
5201-27300/03-1509

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Ramesh et al.

Serial No. 10/716,259

Filed: November 18, 2003

For: IMPROVED MEMORY CELL ARCHITECTURE

§

Group Art Unit: 2827
Examiner: Thong Quoc Le

Atty. Dkt. No. 5201-27300 (03-1509)

I hereby certify that this correspondence is being transmitted via facsimile or deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on the date indicated below:

7/25/05
Date

Pamela Gerik

DECLARATION UNDER 37 C.F.R. 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

We, Ruggero Castagnetti, Ramnath Ventatraman, and Subramanian Ramesh, hereby declare and state that:

1. We are the co-inventors of the above-identified patent application, Serial No. 10/716,259, filed November 18, 2003.

2. We have been informed that in the present application, certain claims have been rejected on reference to U.S. Patent No. 6,847,577 by Ishiguro, issued January 25, 2005 and filed November 12, 2003.

CONCEPTION

3. As set forth in more detail below, we conceived the subject matter claimed in the present application within the United States before November 12, 2003. The subject matter includes an improved memory cell architecture, and in particular, includes a contact structure (such as a bit line, power or ground contact) that is shared unequally between two vertically adjacent memory cells. In accordance with a

particular aspect of the invention, the shared contact structure is formed proximate to a boundary between a memory cell and a vertically adjacent memory cell, such that the shared contact structure is formed: i) completely within the memory cell on one side of the boundary, ii) completely within the vertically adjacent memory cell on an opposite side of the boundary, or iii) formed at the boundary, such that unequal portions of the shared contact structure are formed on either side of the boundary.

4. Exhibit A attached hereto is a true and correct copy of the invention disclosure consisting of ten (10) pages which evidences our conception date before November 12, 2003. For example, a description of a shared contact structure formed completely on one side, or completely on an opposite side, of a boundary between two vertically adjacent memory cells may be found in the invention disclosure, page 3 of 6. Additional description for the contact structure being shared unequally at the boundary may be found on the same page, as well as on page 4 of 6 (which shows the shared BLA and BLNA contacts being unequally shared between two memory cells) and on page 2 of 2 of addendum to the invention disclosure. The invention disclosure is only one example of an earlier conception date of our invention set forth in the claims of our captioned patent application.

REDUCTION TO PRACTICE AND DILIGENCE

10. From at least a time prior to November 12, 2003 through the filing of the application on November 18, 2003, plans were undertaken to prepare the captioned patent application, which was commissioned to Kevin Daffer at Conley, Rose & Tayon, P.C. We did not abandon, suppress, or conceal the ideas set forth in the claimed invention during at least the time beginning prior to November 12, 2003 through the filing of the application on November 18, 2003.

11. Upon information and belief, it is our informed understanding that diligence in reducing the invention to practice was therefore maintained from at least as early as November 12, 2003 through the filing of the application on November 18, 2003.

12. We hereby declare that all statements made herein of our own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 7/14/2005

Ruggero Castagnetti

Date: 7/14/2005

Ramnath Ventatraman

Date: 7/14/05

Subramanian Ramesh

LSI LOGIC CONFIDENTIAL

Patent Docket Number - 03-1509 - Dual Port SRAM Bitcell Architecture
- Invention Disclosure Acknowledgement - Ramnath Venkatraman - ramnathv@lsil.com

Title:	Dual Port SRAM Bitcell Architecture		
Inventor(s)			
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Dates			
Conception	[redacted]	Reduction to practice :	
Disclosure of invention			
Sale or offer for sale of invention			
Use of invention			

Background of invention

Existing problems	Many dual port SRAM bitcell designs (that are commonly reported in the industry) have layouts that have shortcomings with respect to density, performance and robustness. Density is directly related to the area of the bitcell. The performance of the bitcell directly impacts the memory compiler performance and is largely a function of the cell current and the intrinsic capacitances (such as bitline and wordline cap). In addition, dual port cell performance is also impacted by factors such as capacitive coupling between bitlines. Design robustness is key to manufacturability and requires knowledge of the process-limitations. The invention described here is a dual port SRAM bitcell architecture that delivers excellent density, performance and robustness.
Existing solutions to these problems	There are many layouts that have been reported in the industry. To our knowledge the dual port SRAM cell architecture that we are proposing offers the best combination of density, performance and robustness in manufacturing. Note that some aspects of this layout have been used in the dual port cells used in Gflx within LSI Logic. The Gflx SRAM technology was qualified in [redacted]. Please see enclosed document.
Disadvantages of existing solutions	Many of the existing solutions have architectures which lead to cell sizes that are too large or have performance issues. The performance issues can arise from smaller device sizes that are can be fit into the design compared to that in the proposed bitcell architecture. They also arise from higher bitline and wordline capacitances which are also bitcell design-specific. For example, a higher bitline capacitance is associated with the positioning of the bitlines at higher metal levels. Existing solutions also fail to address the importance of not having interport coupling for both bitlines and wordlines. Please see enclosed document.

I/We believe myself (ourselves) to be the first and original inventor(s) of this invention, which was developed during the course of employment. I/We submit this invention disclosure in confidence to attorneys of the LSI Logic IP Law Dept. for the purpose of obtaining a legal opinion and/or advice as to availability of patent, trade secret, and/or copyright protection related to the material contained within.

Inventor(s)		Witnessess who have read and understood the invention	Witness #1
Date			Date
			Witness #2
			Date

LSI LOGIC CONFIDENTIAL

Patent Docket Number - 03-1509 - Dual Port SRAM Bitcell Architecture
- Invention Disclosure Acknowledgement - Ramnath Venkatraman - ramnathv@lsil.com

Description of invention

Details of invention	Please see enclosed document for details of dual port bitcell architecture.
Features of invention	Please see enclosed document.
Advantages of invention	Please see enclosed document
Alternate ways to make or use invention	The invention is very specific with respect to the described layout. Many features features such as bitline location, spacing of port A and port B bitlines with Vss lines in between, as well as reducing coupling between port A and port B wordlines is described. In addition, certain layout specific features such as the use of features that do not mirror exactly at the cell boundary are also key (please see enclosed document for details) to achieving the smaller bitcell size.

Other

Prior Art:	Raszka, J., U.S. Patent 6084826, Dual Port Memory Device with Vertical Shielding
Third party:issues	As noted above, some aspects of the cell design proposed in this invention disclosure have been used in the dual port SRAM bitcells used in Gflx. These bitcells have been processed successfully at TSMC as part of the Gflx LSI-TSMC JDP and have been recently qualified. No products containing such cells have been shipped to customers.

[redacted]

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

I/We believe myself (ourselves) to be the first and original inventor(s) of this invention, which was developed during the course of employment. I/We submit this invention disclosure in confidence to attorneys of the LSI Logic IP Law Dept. for the purpose of obtaining a legal opinion and/or advice as to availability of patent, trade secret, and/or copyright protection related to the material contained within.

Inventor(s)	Witnessess who have read and understood the invention	Witness #1	Witness #2
Date		Date	Date

Dual Port SRAM Bitcell Architecture

Ramnath Venkatraman, Ruggero Castagnetti and Shiva Ramesh

Introduction:

Dual Port SRAMs allow two independent devices (such as a CPU and disk controller or two different CPUs) to have simultaneous read and/or write access to the same memory. Such memories are being used extensively in SoCs. The simultaneous access requires the use of two separate ports, named 'port A' and 'port B' in this document. Figure 1 shows the circuit for a commonly used dual port 8-Transistor SRAM cell. The storage nodes SN1 and SN2 are accessible through two wordlines, WLA and WLB, each wordline being specific to the pertinent port that is being used to read or write the data. Due to the presence of 2 ports, there are two pairs of bitlines named (BLA/BLNA and BLB/BLNB) as shown in Figure 1.

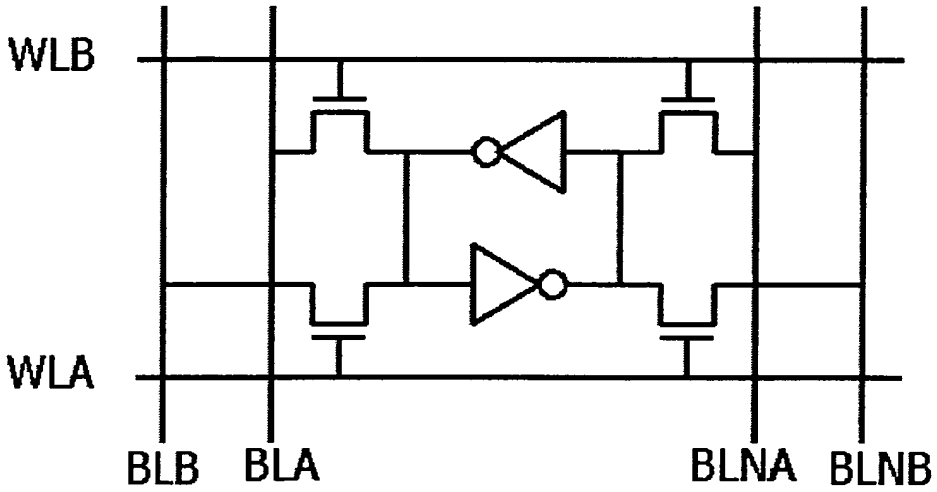


Figure 1: Schematic of a 8-T Dual Port SRAM Cell.

A memory device utilizing such a cell typically has two sets of decoding, control and I/O circuitry, one for each port. This disclosure is concerned with features pertaining to the layout architecture of a dual port cell. Many of these features have already been used by LSI Logic in the dual port cells employed in the 0.13 um (Gflx) generation. This dual port cell architecture is also targeted for G90 and future technology generations.

Dual Port Cell Design Considerations

There are some criteria for design of a dual port cell that are very similar to that for a single port cell.

a) Cell Current: this is maximized by choice of device sizes that can be accommodated in the bitcell layout. Generally, for a given set of implants in the process flow, the higher the size of the NMOS devices within the cell, the higher the cell current. In a dual port cell, the performance of the cell is limited in the situation when both ports are accessed at the same time – therefore, the choice of device sizes is determined taking this scenario into consideration .

b) Cell (beta) ratio: For a dual port cell, the ratio of the pulldown to the pass device drive (proportional to W/L) needs to be twice as high as in a single port cell (due to cell stability restrictions when both ports are being accessed for reading from the same cell).

c) Location of bitlines: it is important that the bitlines be present at the lowest possible metal level (metal 2 or below) due to considerations of allowing extraneous routing signals on top of the memory array at metal 4 and thereby reducing chip level congestion.

There are other criteria for the design of a dual port cell that need to be considered over and above those for a single port cell design.

d) A very important consideration in the design of a dual port cell is interport coupling. For instance, when a particular cell is read using port A bitlines and concurrently, another cell within the same column is being written to using port B bitlines, then the voltage (charge) induced by the port B bitlines on the port A bitlines due to capacitive coupling can impact the bitline separation of the port A bitlines. This can cause a loss in performance of the memory device as a whole or worse, lead to errors in reading the data. A similar event can be imagined when port A and port B bitlines are simultaneously used to access two different cells within the same column - the data state of the cells being accessed can be easily conceived to be such that the separation between the pairs of the port A and port B bitlines are mutually slowed down by the capacitive coupling between them. Therefore, it is important that in a dual port cell, the bitlines for the two ports are capacitively isolated from each other. The insertion of Vss or Vdd lines between the port A and port B bitlines minimizes their mutual coupling. At the same time, it is important that all of the bitlines be present at the lowest possible metal level as stated above. Patent #6,084,820 assigned to Virage Logic ('Dual port Memory Device with Vertial Shielding') addresses the importance shielding between the bitlines of the two ports – however, in this patent the shielding is accomplished by positioning the bitlines at different metal layers and additionally using a vertical shielding layer.

e) Vertical Vss: Due to the fact that upon assertion of both ports along a given row in an array, dual port cells can source twice as much current into the Vss line, it is crucial to make sure that an adequate Vss grid is present within the memory array to reduce the 'floating-up' of the Vss node within the memory cells. The best solution is to have one or more Vss metal lines running vertically within each memory cell and if possible cross-link these vertical lines with horizontal metal lines at a higher metal level.

Lastly it is also important to reduce coupling between the wordlines of port A and port B. This is to prevent unnecessary voltage spikes in either of the wordlines (when wordlines of both ports are asserted concurrently) which can cause increased leakage and/or unwanted upsetting of data in some of the memory cells in the array. Also, since the two ports are operated independently of each other, it is quite possible that while one of the wordlines (say port A wordline) is ramping up in voltage, the other wordline (port B wordline) is ramping down towards Vss. In such a situation any significant capacitive coupling between the wordlines can lead to a delay in turning on the WL as well as in the WL-to-bitline separation time.

Details of Invention

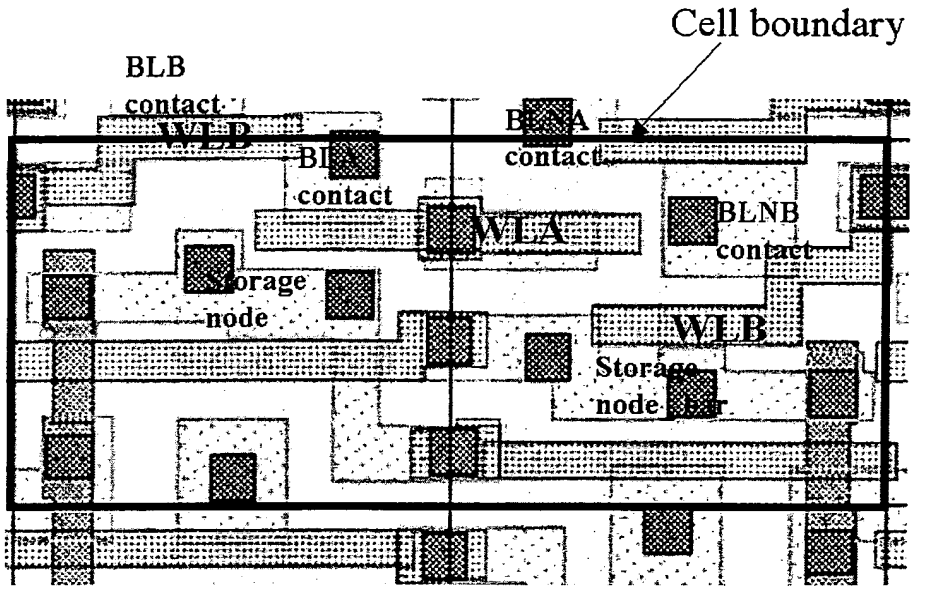
This invention relates to achieving the above mentioned criteria with in our opinion new SRAM dual-port design architecture. The layout shown in Figures 2a, 2b and 2c satisfies all of the above criteria. Most of the features of the cell architecture described above have been proven out successfully in Gflx for 211HD and 222HS compilers. Note that the cell aspect ratio, i.e. the ratio between the height of the cell and the width of the cell is smaller than 1. This has an advantage as the bitline length is minimized, resulting in reduced RC delay and improved memory performance.

Figure 2a shows the layout for island, poly, contact and metal 1. All transistors in this invention are formed in the same direction. This can have an advantage if in case a systematic mismatch exists between transistors that are formed perpendicular to each other. Furthermore, the island features form mostly a straight line thus improving ease of patterning and control.

In state of the art SRAM cell designs all nodes that are shared between neighboring cells are exactly mirrored at the cell boundary. In other words, if a contact is shared between to adjacent cells then that specific contact lies exactly with half side in one cell and with the other half in the adjacent cell. Hence, the cell boundary forms the exact mirror line through the shared node. In our dual-port SRAM cell design the cell boundary does not form an exact mirror line. To use the previous example, in our case, some shared contacts may fully reside within one cell boundary, while other contacts may fully reside in the adjacent cell. Only through the proper mirroring and rotation of multiple cells within an array, the correct cell pattern is reproduced. The uniqueness of this mirroring technique results in a compact layout while incorporating the maximum possible device sizes within the layout to give the best cell performance.

Figure 2b shows the layout with metal 1, via 1 and metal 2. As noted earlier, the arrangement of the bitlines and Vss is such that port A and port B bitlines are well shielded from each other by the use of vertical Vss lines. The arrangement of the bitlines and Vss is as follows: BLB, VSS, BLA, BLNA, VSS, BLNB. It is also noted that the

presence of two vertical Vss lines within each cell which are cross-linked at metal 3 with a horizontal Vss line provides an excellent Vss grid. Figure 2c shows the layout with metal 2, via 2 and metal 3. Here the arrangement of the port A and port B wordlines is such that they are well shielded from each other by Vss and Vdd lines. Furthermore, the presence of the horizontal Vss metal 3 lines adds to the robustness of the Vss grid in the memory array.



Yellow = N+ Island, Blue = P+ island
Pink = Poly, Black = contact, Bluish Green = Metal 1

Figure 2a: Layout of dual port cell with island, poly, contact and metal 1 . Note that even though the layout utilizes bitline contacts and Vss contacts that are shared by adjacent cells, these contacts are not symmetrically placed with respect to the cell edge. However, the intended array pattern is produced when the cell is rotated/mirrored appropriately. This offers a much more compact layout pattern while maximizing cell performance.

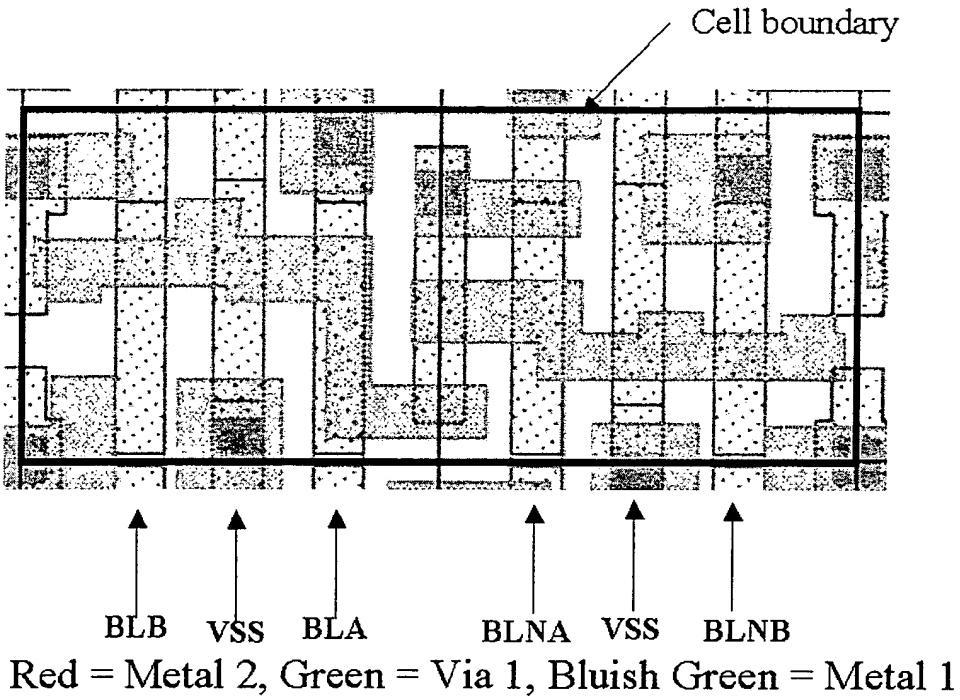
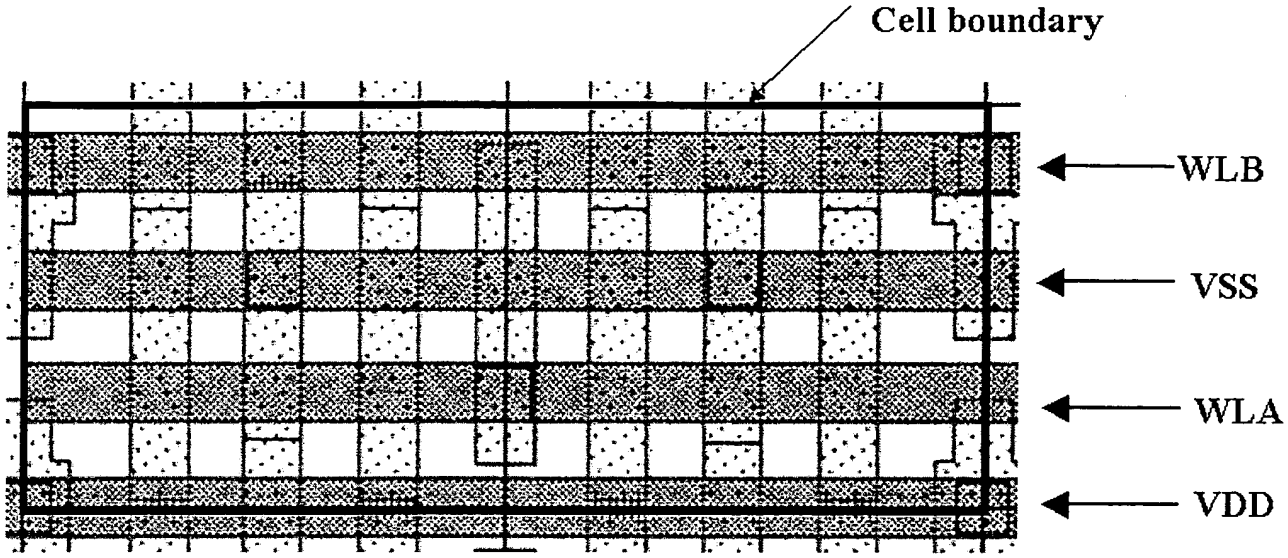


Figure 2b: Layout of dual port cell with metal 1, poly and metal 2. The key advantages illustrated are i) short bitlines, ii) bitlines at metal 2, iii) vertical Vss iv) shielding between port A and port B bitlines through insertion of Vss lines.



Red = Metal 2, Blue = Via 2, Blue = Metal 3

Figure 2c: Layout of dual port cell with metal 2, via 2 and metal 3. Key advantages illustrated are i) Shielding between WLA and WLB is achieved by the introduction of horizontal Vss line at metal 3 and ii) improved Vss grid to supplement vertical Vss lines shown in Figure 2b.

Addendum to Disclosure docket no. 03-1509
(as per suggestion by reviewer)

The key features of our dual port cell layout that offers excellent density and performance advantages are as follows. Comparison is also made to features of a cell described in Patent no 6,084,820 "Dual Port Memory Device with Vertical Shielding".

1) The dual port cell described in this invention has an overall cell dimension aspect ratio (height to width ratio) of less than 1. This implies relatively short bitlines and therefore offers the advantage of a low bitline capacitance value (for improved performance). The prior art does not specify this detail.

2) All transistors in the bitcell are formed in the same direction. This is advantageous in case there is a systematic difference between transistors that are perpendicular to each other and therefore can lead to unintended differences between the performance of the two ports. The prior art does not specify this detail.

3) All bitlines are at metal 2 (Figure 2b). This has two advantages: firstly, low bitline capacitance compared to designs where bitlines are at higher metal levels, and secondly, this allows for significant advantages with respect to allowing extraneous routing signals on top of the memory array and thereby reduce chip level congestion. In patent 6,086,820 the authors describe using one set of bitlines specific to one port being disposed on one metal level and the other set of bitlines specific to the other port being disposed on another metal level. There is no concern addressing the disadvantage of having bitlines at higher metal levels.

4) Each cell has a vertical Vss line at metal 2, running in the same direction as the bitlines (Figure 2b). The presence of a vertical Vss line within the cell is very important from the point of view of minimizing any local increase in the voltage of the Vss line within the memory array (thus minimizing performance loss as well as cell stability loss). This issue is especially important for dual port cells due to the higher amount of current that is sourced into the Vss line every time a read operation is performed on both ports A and B. This is not addressed in patent 6,084,820.

5) Port A and Port B metal 2 bitlines are separated by metal 2 Vss. This minimizes interport coupling for bitlines. This shielding is an extremely important feature to achieve maximum performance for the dual port memory. In patent 6,084,820, to achieve shielding, the bitlines corresponding to the two ports are placed in different metal levels, which are separated by another metal level used as a shielding layer. The shielding layer serves the purpose of minimizing interport

coupling. However, due to the fact that this approach places one set of bitlines at a higher metal level (such as metal 4), there are serious adverse consequences of having routing restrictions.

6) Port A and Port B word lines run horizontally at metal 3 (Figure 2c) and are connected to the port A and port B pass gate poly segments. Each pass gate poly segment is shared by two pass transistors. These two transistors sharing the common poly gate segment can be within the same bitcell (as with WLA shown in Figure 2a) or can be shared by two adjacent cells (as with WLB shown in Figure 2a). This detail is not discussed in the prior art.

7) Port A and Port B word lines which are at metal 3 are separated by a horizontal metal 3 Vss line (Figure 2c). This is advantageous from the point of view of reducing interport word line coupling (and thereby improving overall memory performance). This detail is not discussed in the prior art

8) The presence of a horizontal Vss line at metal 3 in addition to the vertical Vss line at metal 2. This is advantageous to provide a more robust Vss grid and therefore minimize local increases in the voltage of the Vss connections (as pointed out in 4)).

9) The presence of a horizontal Vdd line within the cell at metal 3, which is shared between two adjacent cells, is a feature of this layout.

10) A special feature of the layout is the use of bitline contacts and Vss contacts that are not mirrored symmetrically across the cell boundary. However, the left and right halves of the cells are designed such that when the cell is mirrored vertically & horizontally and placed adjacently, it will result in the bitline contacts and Vss contacts being shared by the two adjacent vertical bits. This feature results in a reduction of the cell dimension in the vertical direction and therefore results in a lower cell size and higher memory performance & density.